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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/477,099	01/04/2000	FREDERICK S. DUNLAP	P04056	8711

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EXAMINER	
BETIT, JACOB F	

ART UNIT	PAPER NUMBER
2164	

DATE MAILED: 12/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/477,099	DUNLAP ET AL.	
	Examiner	Art Unit	
	Jacob F. Betit	2164	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *24 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

SAM RIMELL
PRIMARY EXAMINER

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Remarks

1. In response to communications filed on 24-May-2004, claim 11 is amended and claims 21-22 are cancelled per applicant's request. Claims 1-20 are presently pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-9 and 11-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsumura et al. (U.S. patent No. 5,365,475).

As to claim 1, Matsumura et al. teaches a static random access memory (SRAM) device capable of storing a program that is accessible when said SRAM device is powered up, said SRAM device comprising a plurality of storage cells (see column 1, lines 15-19), each of said storage cells comprising:

a data latch having a first input/output (I/O) line and a second I/O line (see figure 3, *BL* and $\overline{BL}$), said data latch comprising:

a first inverter having an input coupled to said first I/O line and an output coupled to said second I/O line (see figure 3, NA); and

a second inverter having an input coupled to said second I/O line and an output coupled to said first I/O line (see figure 3, NB); and

a biasing circuit capable of forcing at least one of said first and second I/O lines to a known logic state when power is applied to said SRAM device, wherein said known logic state comprises a portion of said program (see figure 3, G_1, G_2, V_1, and V_2).

As to claim 11, Matsumura et al. teaches a data processor comprising a central processing unit (CPU) capable of executing a boot-up program when power is applied to said CPU (see figure 15), said CPU comprising:

a static random access memory (SRAM) device capable of storing said boot-up program, said SRAM device comprising a plurality of storage cells capable of storing bits of said boot-up program (see column 1, lines 15-19), each of said storage cells comprising:

a data latch having an input and an output (see figure 3, BL and $\overline{BL}$), said data latch comprising:

a first inverter having an input coupled to said first I/O line and an output coupled to said second I/O line (see figure 3, NA); and

a second inverter having an input coupled to said second I/O line and an output coupled to said first I/O line (see figure 3, NB); and

a biasing circuit capable of forcing at least one of said first and second I/O lines to a known logic state when power is applied to said SRAM device (see figure 3, G_1, G_2, V_1, and

V_2), wherein said known logic state comprises a portion of said boot-up program (see column 11, lines 3-17).

As to claims 2 and 12, Matsumura et al. teaches wherein said biasing circuit initially applies power only to said first inverter (see column 7, line 62 through column 8, line 36).

As to claims 3 and 13, Matsumura et al. teaches wherein said initial application of power only to said first inverter forces said first inverter output to a Logic 1 state (see column 7, line 62 through column 8, line 36).

As to claims 4 and 14, Matsumura et al. teaches wherein said biasing circuit subsequently applies power to said second inverter (see column 9, lines 8-14).

As to claims 5 and 15, Matsumura et al. teaches wherein said subsequent application of power to said second inverter forces said second inverter output to a Logic 0 state (see column 9, lines 8-14).

As to claims 6 and 16, Matsumura et al. teaches wherein said biasing circuit initially applies power only to said second inverter (see column 7, line 62 through column 8, line 36).

As to claims 7 and 17, Matsumura et al. teaches wherein said initial application of power only to said second inverter forces said second inverter output to a Logic 1 state (see column 7, line 62 through column 8, line 36).

As to claims 8 and 18, Matsumura et al. teaches wherein said biasing circuit subsequently applies power to said first inverter (see column 9, lines 8-14).

As to claims 9 and 19, Matsumura et al. teaches wherein said subsequent application of power to said first inverter forces said first inverter output to a Logic 1 state (see column 9, lines 8-14).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 10 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumura et al. (U.S. patent No. 5,365,475) in view of Shimazu et al. (U.S. patent No. 4,777,623).

As to claims 10 and 20, Matsumura et al. does not teach wherein said biasing circuit comprises a grounding circuit selectively connected by a programmable connect to one of said

first inverter output and said second inverter output, wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device, thereby grounding one of said first inverter output and said second inverter output and forcing said second 1/O line to said known logic state.

Shimazu et al. teaches wherein said biasing circuit comprises a grounding circuit selectively connected by a programmable connect to one of said first inverter output and said second inverter output, wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device, thereby grounding one of said first inverter output and said second inverter output and forcing said second 1/O line to said known logic state (see column 3, line 65 through column 4, line 14).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Matsumura et al. to include said biasing circuit comprises a grounding circuit selectively connected by a programmable connect to one of said first inverter output and said second inverter output, wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device, thereby grounding one of said first inverter output and said second inverter output and forcing said second 1/O line to said known logic state.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Matsumura et al. by the teachings of Shimazu et al. because said biasing circuit comprises a grounding circuit selectively connected by a programmable connect to one of said first inverter output and said second inverter output, wherein said grounding circuit is temporarily enabled after power is applied to said SRAM

device, thereby grounding one of said first inverter output and said second inverter output and forcing said second I/O line to said known logic state would allow the device to be set or reset (see Shimazu et al., column 1, lines 7-10).

Response to Arguments

6. Applicant's arguments filed 24-May-2004 have been fully considered but they are not found to be persuasive.

In response to the applicant's arguments that "Matsumura ... fails to mention the storage of a program accessible when the memory device is powered up", the arguments have been fully considered but are not deemed persuasive because Matsumura teaches using the memory device as a ROM to store programs from the manufacture (see column 11, lines 3-37). It is inherent that a ROM would contain the program when it is powered on.

In response to the applicant's arguments that "Matsumura fails to disclose the limitations of each of a plurality of storage cells of the SRAM device comprising a biasing circuit capable of forcing at least one of first and second I/O lines to a known logic state when power is applied to the SRAM device, wherein the known logic state comprises a portion of the program", the arguments have been fully considered, but are not deemed persuasive because Matsumura teaches if the memory circuit is configured as shown in figure 5A it is configured to be a ROM cell storing the data "0" and if the memory circuit is configured as shown in figure 5B it is configured to be a ROM cell storing the data "1" (see column 7, lines 15-59). He goes on to

teach the memory cell of 106b storing programs from the manufacturer using his disclosed invention and also being used as a RAM during user operation (see column 11, lines 2-17). Therefore Matsumura teaches these limitations.

In response to the applicant's arguments that "Shimazu fails [to] disclose a grounding circuit selectively connected to one of a first inverter output and a second inverter output", the arguments have been fully considered, but are not deemed persuasive because Shimazu teaches a MOS transistor which has sufficient driving capability to pull down the level of the input data line to "0" or ground (see column 4, lines 11-14). This is a programmable connect that selectively connects a "grounding circuit" to an inverter output. The claim limitations only require a grounding circuit to be selectively connected to one of the first or second inverter output, and therefore Shimazu teaches the limitations of the claim.

In response to the applicant's arguments that "Shimazu fails to disclose a programmable connect for selectively connecting the grounding circuit to one of the first and second inverter outputs", the arguments have been fully considered, but are not deemed persuasive because Shimazu teaches a MOS transistor which has sufficient driving capability to pull down the level of the input data line to "0" or ground (see column 4, lines 11-14). This is a programmable connect that selectively connects a grounding circuit to an inverter output. The claim limitations only require a grounding circuit to be selectively connected to one of the first or second inverter output, and therefore Shimazu teaches the limitations of the claim.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob F. Betit whose telephone number is (571) 272-4075. The examiner can normally be reached on Monday through Friday 9 am to 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici can be reached on (571) 272-4083. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jfb
7 Dec 2004

SAM RIMELL
PRIMARY EXAMINER